

EAST - [10800792.wsp:1]

File View Edit Tools Window Help

☐ Drafts
☐ BRS: memory and (storage near node)
☐ Pending
☒ Active
☐ L1: (271) scalable near two-transistor near memory scalable near two near transistor near memory...
☐ L2: (9) scalable near two-transistor near memory scalable near two near transistor near memory ne...
☐ L3: (12) scalable near two-transistor near memory scalable near two near transistor near memory
☐ L4: (5) memory and (memory near node storage near node) and tunnel near junction near barrier and...
☐ L5: (9) memory and (memory near node storage near node) and tunnel near junction near barrier and...
☐ L6: (211) memory and (memory near node storage near node) and barrier and (data near line data ne...
☐ L7: (43) memory and (memory near node storage near node) and (tunnel near10 barrier) and (data ne...
☐ Failed
☐ Saved
☐ Favorites
☐ Tagged (0)
☐ UDC
☐ Queue
☐ Trash

Search List Browse Queue Clear
 DBs US-PGPUB: USPAT: Plurals
 Default operator: OR Highlight all hit terms initially

memory and (memory near node storage near node) and (tunnel near10 barrier) and (data near line data near electrode) and gate and (dielectric insulatS3)

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050156225 A1	20050721	26	Methods of fabricating semiconductor devices with scalable two transistor memory cells	257/316	438/266
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20050127429 A1	20050616	55	Semiconductor nonvolatile memory device	257/315	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20050030829 A1	20050210	47	Thin film magnetic memory device conducting data write operation by application of a magnetic field	365/232	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20040252576 A1	20041216	22	Semiconductor memory element arrangement	365/232	257/E21.68; 257/E27.103
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20040238974 A1	20041202	26	Scalable two transistor memory devices and methods of fabrication therefor	257/314	257/900
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20040227173 A1	20041118	27	Semiconductor devices with scalable two transistor memory cells and methods of fabricating the same	257/296	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20040170050 A1	20040902	27	Semiconductor integrated circuit device with improved storage MOSFET arrangement	365/149	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20040150022 A1	20040805	25	Semiconductor memory device having a multiple tunnel junction pattern and method of fabricating the same	257/296	257/E27.084
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20040084714 A1	20040506	43	Semiconductor memory device	257/315	257/E21.682; 257/E27.103; 257/E29.308
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20030209739 A1	20031113	43	Vertical semiconductor device with tunnel insulator in current path controlled by gate electrode	257/278	257/E21.629; 257/E27.084; 257/E29.042
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20030205771 A1	20031106	27	Semiconductor memory device and manufacturing method	257/390	257/E27.084; 257/E29.165; 257/E29.242